

74HC574

Octal 3-State Noninverting D Flip-Flop

High-Performance Silicon-Gate CMOS

The 74HC574 is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

Data meeting the set-up time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574 is identical in function to the HC374A but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

Features

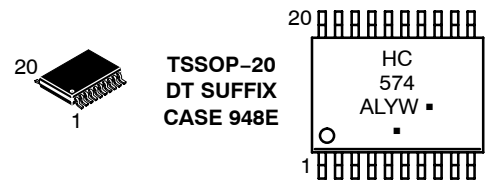
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates
- This is a Pb-Free Device



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MARKING DIAGRAMS



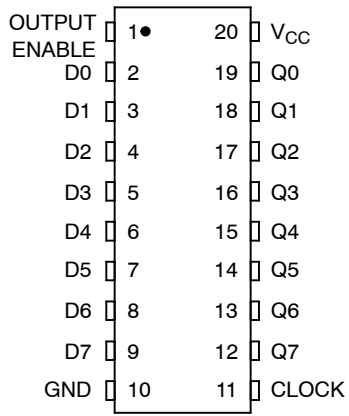
HC574 = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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FUNCTION TABLE

Inputs			Output
OE	Clock	D	Q
L		H	H
L		L	L
L	L,H,	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

Figure 1. Pin Assignment

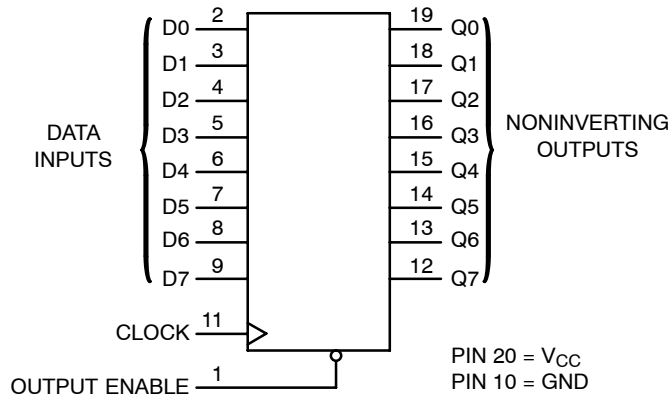


Figure 2. Logic Diagram

Design Criteria	Value	Units
Internal Gate Count*	66.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μ W
Speed Power Product	0.0075	μ J

*Equivalent to a two-input NAND gate.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	- 0.5 to +7.0	V
V _I	DC Input Voltage	- 0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage (Note 1)	- 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 35	mA
I _O	DC Output Sink Current	± 35	mA
I _{CC}	DC Supply Current per Supply Pin	± 75	mA
I _{GND}	DC Ground Current per Ground Pin	± 75	mA
T _{STG}	Storage Temperature Range	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+ 150	°C
θ _{JA}	Thermal Resistance TSSOP	128	°C/W
P _D	Power Dissipation in Still Air at 85°C TSSOP	450	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% - 35%	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3)	>2000 >200	V
I _{Latchup}	Latchup Performance Above V _{CC} and Below GND at 85°C (Note 4)	± 300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to EIA/JESD78.
5. For high frequency or heavy load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _I , V _O	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 3)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

6. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

ORDERING INFORMATION

Device	Package	Shipping [†]
74HC574DTR2G	TSSOP-20*	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} (V)	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V I _{out} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0	2.48	2.34	2.2	V
			4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0	0.26	0.33	0.4	
			4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	± 0.5	± 5.0	± 10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4.0	40	40	μA

7. Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF; Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V _{CC} (V)	Guaranteed Limit			Unit
			-55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3 and 6)	2.0	6.0	4.8	4.0	MHz
		3.0	15	10	8.0	
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 3 and 6)	2.0	160	200	240	ns
		3.0	105	145	190	
		4.5	32	40	48	
		6.0	27	34	41	
t _{P LZ} , t _{P HZ}	Maximum Propagation Delay, Output Enable to Q (Figures 4 and 7)	2.0	150	190	225	ns
		3.0	100	125	150	
		4.5	30	38	45	
		6.0	26	33	38	
t _{P ZL} , t _{P ZH}	Maximum Propagation Delay, Output Enable to Q (Figures 4 and 7)	2.0	140	175	210	ns
		3.0	90	120	140	
		4.5	28	35	42	
		6.0	24	30	36	
t _{TLH} , t _{THL}	Maximum Output Transition Time, any Output (Figures 3 and 6)	2.0	60	75	90	ns
		3.0	27	32	36	
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance		10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance, Output in High-Impedance State		15	15	15	pF

8. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Enabled Output)*	Typical @ 25°C, V _{CC} = 5.0 V		pF
		24		

*Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF; Input t_r = t_f = 6.0 ns)

Symbol	Parameter	Figure	V _{CC} (V)	Guaranteed Limit						Unit
				-55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t _{su}	Minimum Setup Time, Data to Clock	5	2.0	50		65		75		ns
			3.0	40		50		60		
			4.5	10		13		15		
			6.0	9.0		11		13		
t _h	Minimum Hold Time, Clock to Data	5	2.0	5.0		5.0		5.0		ns
			3.0	5.0		5.0		5.0		
			4.5	5.0		5.0		5.0		
			6.0	5.0		5.0		5.0		
t _w	Minimum Pulse Width, Clock	3	2.0	75		95		110		ns
			3.0	60		80		90		
			4.5	15		19		22		
			6.0	13		16		19		
t _p , t _f	Maximum Input Rise and Fall Times	3	2.0		1000		1000		1000	ns
			3.0		800		800		800	
			4.5		500		500		500	
			6.0		400		400		400	

SWITCHING WAVEFORMS

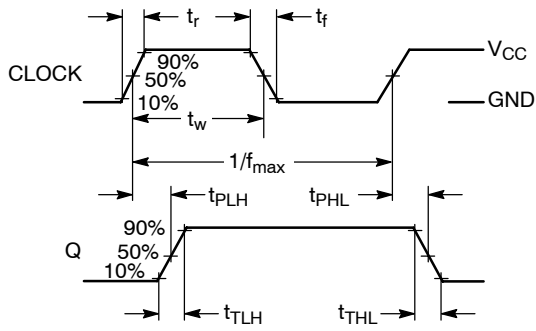


Figure 3.

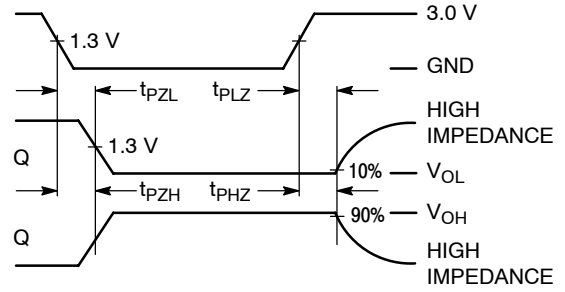


Figure 4.

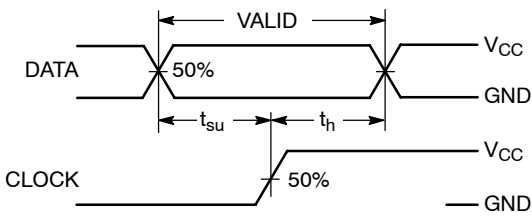
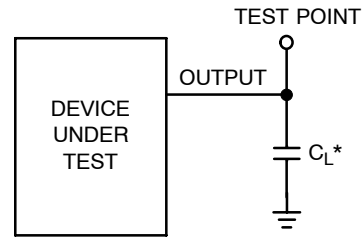
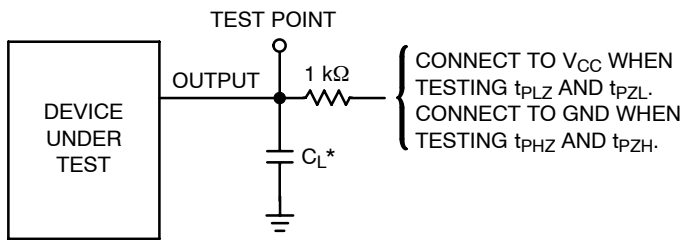


Figure 5.



*Includes all probe and jig capacitance.

Figure 6.



*Includes all probe and jig capacitance.

Figure 7. Test Circuit

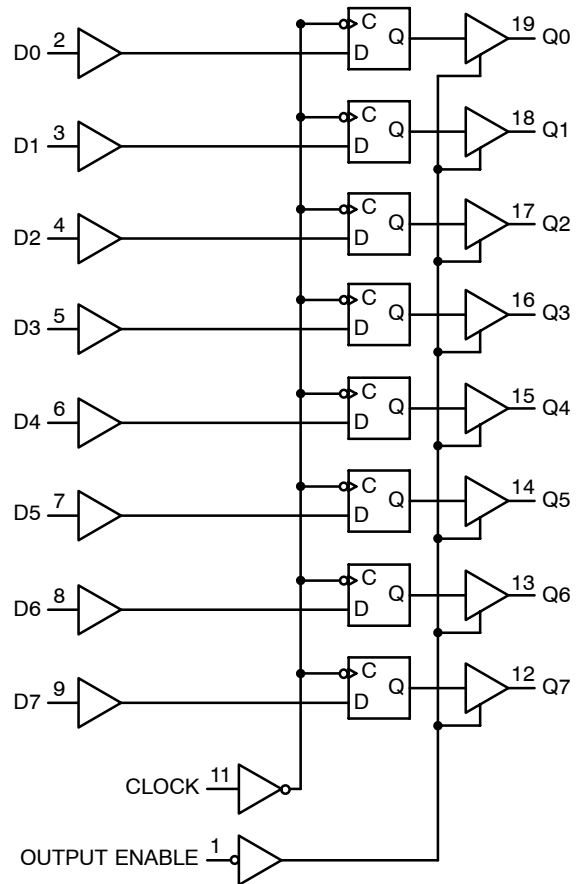
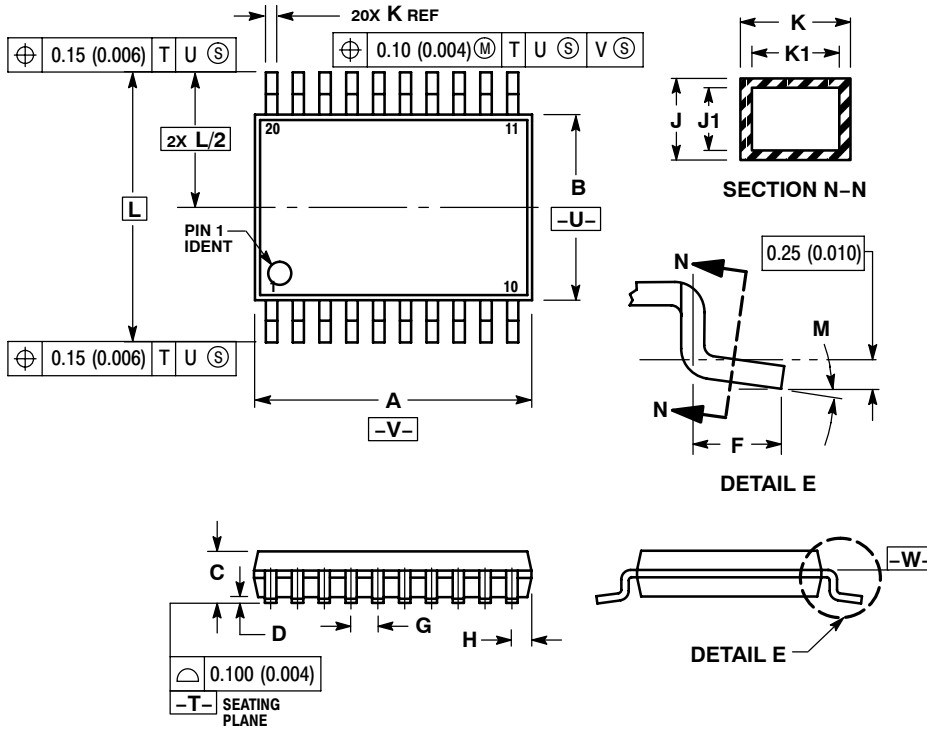


Figure 8. Expanded Logic Diagram

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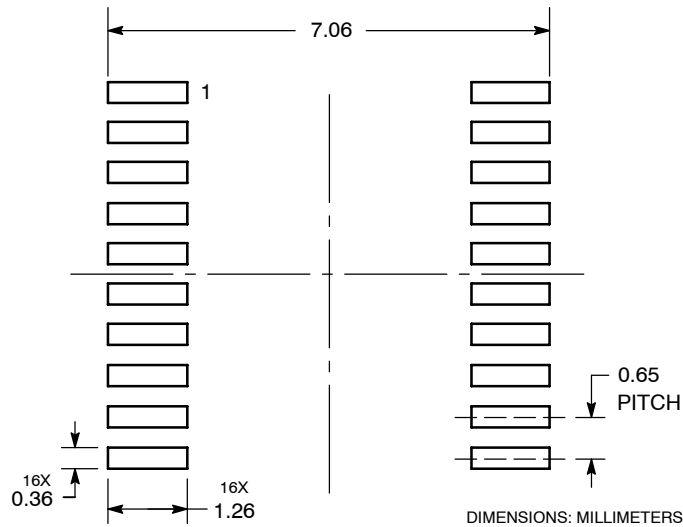
PACKAGE DIMENSIONS

TSSOP-20
CASE 948E-02
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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